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Design the architecture of a 4-bit capacitor DAC. 12.15 A bias generator is required to generate 16 steps from 0 to 100 μA to bias an amplifier. Design a CMOS DAC to do this, assuming the presence of a 50 μA reference current. 12.16 Differential circuits provide good noise immunity and have the advantage of dual rail inputs and outputs.

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Course Overview. N. Weste and D. Harris. Chapter 1.CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed., Addison Wesley, 2011.[pdf | link] Topic 1: Hardware ...

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Neil H. E. Weste (born 1951), is an Australian inventor and engineer, noted for having designed a 2-chip wireless LAN implementation and for authoring the textbook Principles of CMOS VLSI Design. He has worked in many aspects of integrated-circuit design and was a co-founder of Radiata Communications.

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